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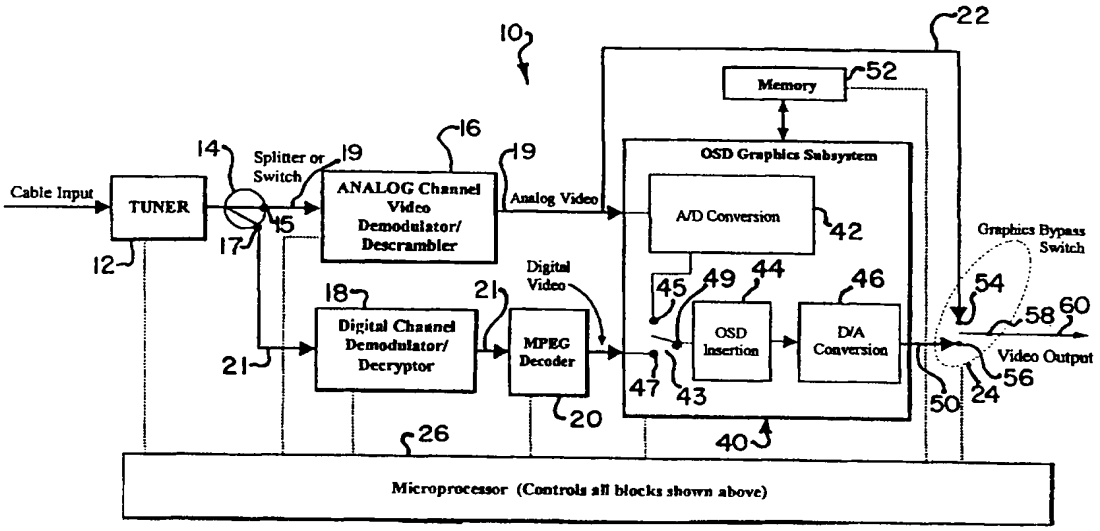
(54) Title: GRAPHICS SUBSYSTEM BYPASS METHOD AND APPARATUS



(57) Abstract: The present invention provides an on-screen graphics (OSD) subsystem for overlaying OSD graphic images onto analog or digital video source signals. The OSD system has a video graphics bypass path (22) and graphics bypass switch (24) for directing an analog video channel around the OSD subsystem during time intervals when the OSD subsystem is not required to insert graphics into the source signal.

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GRAPHICS SUBSYSTEM BYPASS METHOD AND APPARATUS

BACKGROUND

The present invention relates to cable television (CATV) systems. More particularly, the present invention pertains to a method and apparatus for bypassing a digital on-screen display graphics insertion subsystem.

The wide spread use of analog video displays has created a need for displaying graphic images such as alphanumeric characters or other graphics along with analog video data. The graphics are typically laid over a video signal received from a separate remote source such as a broadcast television transmission, a video disk, a video tape or any other video source. Various arrangements are known for overlaying graphic images over a video signal received from such a separate remote video source.

U.S. Patent No. 5,051,817 to Takano discloses a system for superimposing color characters on an input video signal. In this system, a first sync separator separates horizontal sync pulses from the input video signal. These horizontal sync pulses are used by a phase lock loop (PLL) circuit to generate a reference clock signal (P1) that is locked to the horizontal sync pulses of the input video signal. A second sync separator, a timing generator, a burst gate, and a second PLL circuit generate an oscillation output signal that is phase locked to a burst signal of the input video signal. The reference clock signal and the oscillation output signal are used to synchronize a generated character signal with the input video signal. A changeover signal generator generates changeover control signals to output only the input video signal, or the input video signal superimposed with color characters.

U.S. Patent No. 5,541,666 to Zeidler et al. discloses a system for overlaying digital character signals on an analog source signal including a predetermined color sub-carrier which includes a sub-carrier phase locked loop, a digital character generating device, a digital video encoder and a switching device. The subscriber phase locked loop separately generates a color sub-carrier and a system clock signal which are locked to the color sub-carrier of the analog video source system. The digital character generating device detects horizontal and vertical timing of pixel information in the analog video source signal, and generates digital character signals that are to be overlaid in predetermined pixels of the analog video source signal. The digital video encoder is responsive to the color sub-carrier and system clock signals for generating a separate color sub-carrier which is locked to the color sub-carrier of the analog video source signal. The digital video encoder also converts the digital character signals from the digital character generating means into an analog video output signal that includes the color sub-carrier generated in the digital video encoder. The switching means directs the analog video output signal from the digital video encoder or the analog video source signal to an output of this system during times when the digital character is to be overlaid or not overlaid respectively on the analog video source signal.

A problem exists with these techniques in that insertion of digital information into an analog video source may only be required in certain time intervals. The insertion process inherently degrades the video signal. Signal degradation occurs

both during time intervals when digital information is inserted and during time intervals when there is no digital information presented for insertion.

SUMMARY

It is therefore an object of the present invention to provide a method and apparatus for overlaying graphics on video signals and to bypass an OSD graphics subsystem for overlaying the graphics on the video signals during intervals when there are no graphics are presented for overlaying.

These and other objects have been achieved by providing a graphics subsystem for receiving digital video source signals or converting analog video source signals to digital video signals, inserting on screen display (OSD) graphics into the video source signals to form a composite digital signal and converting the composite digital signal to an analog video signal for output to a display. A graphics subsystem bypass circuit is provided for passing inbound analog video source signals directly to the display during intervals when no OSD graphics are present for overlaying.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will now be described by way of example with reference to the accompanying figures of which:

Figure 1 is a block diagram of a system containing a graphics subsystem bypass according to the present invention.

Figure 2 is a flow diagram for the operation of the system in **Figure 1**.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Figure 1 is a block diagram of a settop terminal **10**. The settop terminal **10** contains a tuner **12** coupled to a cable input from a community antenna television (CATV) network. A switch **14** is coupled to the output of the tuner **12**. It should be understood by those reasonably skilled in the art that the switch **14** may optionally be replaced by a splitter. Outputs **15**, **17** of the switch **14** are coupled to an analog video path **19** and a digital video path **21** respectively. An analog channel video demodulator **16** is coupled to the first switch output **15** along the analog video path **19**. It should be understood by those reasonably skilled in the art that the analog channel video demodulator **16** may also optionally include a descrambler in systems where the cable input is a scrambled signal.

A digital channel demodulator **18** is coupled to the second switch output **17** along the digital video path **21**. It should be understood by those reasonably skilled in the art that the digital channel demodulator **18** may optionally include a decryptor for use in systems having encrypted digital information being passing through the

tuner **12.** A motion picture expert group (MPEG) decoder **20** is coupled to the output of the digital channel demodulator **18** within the digital video path **21**. Both the analog video and digital video paths **19**, **21** are coupled to an on-screen display (OSD) graphics subsystem **40**.

The OSD graphics subsystem **40** includes an analog to digital (A/D) convertor **42** coupled to the analog video path **19** and a switch **43** having two inputs **45**, **47**. The inputs **45**, **47** are coupled to the A/D convertor **42** and the MPEG decoder **20** respectively. Also included in the OSD graphics subsystem **40** is an OSD insertion unit **44** coupled to switch output **49**, a digital to analog (D/A) convertor **46**, which is coupled to the OSD insertion unit **44** and an output **50**. The OSD graphics subsystem **40** including the A/D convertor **42**, the switch **43**, the OSD insertion unit **44** and the D/A convertor **46** may comprise a single chip or chip set, for example ATI Technologies Rage Pro and Rage Theatre. It should be recognized that other vendors offer similar chips or chip sets having these functions. Any such suitable chip or chip set having these functions could be utilized.

A graphics bypass switch **24**, having two inputs **56**, **54**, is coupled to the OSD graphics subsystem output **50** and to an OSD bypass path **22**. The bypass path **22** extends from the analog video path **19** to the graphics bypass switch input **54**. A video output **60** is provided from the graphics bypass switch output **58**. Memory **52** is coupled to the OSD graphics subsystem **40**. Additionally, microprocessor **26** is provided for selectively controlling each of the components described above.

Referring to **Figure 2**, general operation of the system 10 of **Figure 1** will now be described. First, an input channel from the tuner **12** is split or switched. Next, a determination is made by the microprocessor **26** whether the channel is digital or analog. If it is a digital channel, demodulation and an MPEG decoding process is initiated through microprocessor control of switch **14** followed by an on-screen display insertion process to insert the OSD information into the digital video input. Following the OSD insertion process a video signal containing both digital video and graphics inserted information is converted to analog at the digital to analog convertor **46** and output to a standard monitor. Returning to the top of **Figure 2**, if the channel is analog it is directed along the analog path **19** through microprocessor control of switch **14**. It is passed then through the OSD graphics subsystem, or a bypass is activated by the microprocessor **26** to redirect the demodulated input channel directly to the video output **60** for display on a standard monitor.

System operation will now be described in greater detail with reference to **Figure 1**. The memory **52** contains OSD graphics image information in digital format which is stored there by the microprocessor **26**. It should be understood, that this information may be modified by the microprocessor **26** in order to display different OSD graphics images on the video output **60**. The settop terminal **10** receives a cable input from a CATV network via the tuner **12**, which selects a desired channel from the cable input. Based upon whether the selected channel is digital or analog, the switch **14** directs the selected channel to the analog channel

video demodulator **16** through the analog video path **19** or to a digital channel demodulator **18** through the digital video path **21**. These will be referred to as the digital channel and the analog channel. The digital channel typically contains MPEG compressed video, while the analog channel typically contains picture signals such as NTSC or PAL or other standard signals. It should be understood however that each of these channels may carry other information content in the form of analog and digital signals.

The analog channel video demodulator **16** serves to demodulate the analog channel and also optionally serves to descramble any scrambled analog video signal. A demodulated analog video signal is fed from the analog channel video demodulator **16** along the analog video path **19** to both the graphics bypass path **22** and the OSD graphics subsystem **40**.

The digital channel demodulator **18** serves to demodulate the digital channel and may optionally de-encrypt any digitally encrypted signal. A demodulated digital signal is fed from the digital channel demodulator **18** along the digital video path **21** to the MPEG decoder **20**. It should be understood that while the decoder **20** is shown as an MPEG decoder, other digital compression techniques may be utilized and decoded accordingly. The MPEG decoder **20** serves to decode the MPEG encoded signal into a pure digital video signal, which is fed into the OSD graphics subsystem **40**.

The digital video signal coming from the MPEG decoder **20** is fed to the second switch input **47**. The switch **43** is operated by the microprocessor **26** to feed

the A/D converted video signal to the OSD insertion unit **44** during selected time intervals when the tuner **12** is tuned to an analog channel. The switch **43** is also operated by the microprocessor **26** to feed the digital video signal coming from the MPEG decoder **20** to the OSD insertion unit **44** during other selected time intervals when the tuner **12** is tuned to a digital channel. Depending upon the switch's position, the OSD insertion unit **44** combines the digital video signal from the digital video path **21** or the digitized analog video signal from the analog video path **19** with the desired OSD graphics previously stored in memory **52**. The combined or composite signal is then fed to the D/A convertor **46** for conversion to an analog signal, which contains digital or analog video source signals from the tuner **12** and OSD graphics inserted from memory **52**. The memory **52** also serves to temporarily store A/D information, D/A information and data for the OSD insertion unit **44**.

The graphics bypass switch **24** is controlled by the microprocessor **26** to switch the video output **60** between the graphics bypass path **22** and the OSD graphics subsystem output **50**. It should be appreciated that the OSD graphics subsystem, by use of A/D and D/A convertors **42**, **46**, degrades the signal quality at the video output **60**. Therefore, when there is no OSD graphics present for combination with the analog channel, the bypass path **22** serves to pass the analog video signal directly to the video output **60** without any degradation that would otherwise be experienced through the OSD graphics subsystem **40**.

An advantage of the present invention is that during intervals when OSD graphics is not required for combination with an analog signal, the analog video

signal may be passed directly to a video output **60** without degradation experienced through signal conversions in the OSD graphics subsystem **40**.

* * *

What is claimed is:

1. A video graphics subsystem for use in a video terminal comprising:

a digital video input configured to receive a digital signal;

an analog video input configured to receive an analog video signal;

an analog to digital converter having a digital output and an input for receiving the analog video signal from the analog video input;

an on-screen display insertion unit having a digital output and an input selectively coupled to both the digital video input or the digital output of the analog to digital converter;

a digital to analog converter having an analog output and a digital input coupled to the digital output of the on-screen display unit; and

a bypass extending from the analog video input through a switch connected to the analog output.

2. The video graphics subsystem recited in claim 1 further comprising a second switch having inputs each coupled to the digital video input and the analog video input and an output coupled to the on-screen display insertion unit input.

3. The video graphics subsystem recited in claim 1 further comprising a memory for storing information from the analog to digital and digital to analog convertors.

4. The video graphics subsystem recited in claim 3 further comprising a microprocessor for generating and storing a graphic in the memory.

5. The video graphics subsystem recited in claim 4 wherein the on-screen display insertion unit receives the graphic and combines the graphic with a signal applied to its input.

6. The video graphics subsystem recited in claim 5 wherein the microprocessor directs a signal on the analog video input to the bypass during intervals when no graphic is required.

7. A video graphics subsystem comprising:

a first converting means for converting an inbound analog video signal to a digital video signal;

insertion means for combining the digital video signal with a digital graphic to form a composite digital video signal;

a second converting means for converting the composite digital video signal to a composite analog video signal; and

bypass means for bypassing the first converting means, the insertion means and the second converting means.

8. The video graphics subsystem recited in claim 7 wherein the bypass means comprises a bypass switch.

9. The video graphics subsystem recited in claim 8 wherein the bypass switch is controllable in response to sensing the requirement of a digital graphic.

10. The video graphics subsystem recited in claim 9 further comprising a microprocessor for sensing the requirement of a digital graphic and controlling the switch.

11. A method for inserting intermittent graphics signals into an analog video signal comprising the steps of:

a) converting the analog video signal to a digital video signal;

b) inserting at least one of the intermittent graphics signals into the digital video signal forming a composite digital video signal;

c) converting the composite digital video signal to a composite analog video signal; and

d) bypassing steps a, b, and c during time intervals when the intermittent graphics signals are not present.

12. The method of claim 11 further comprising the step of generating a digital representation of an image to form the graphics signals.

13. The method of claim 12 further comprising the step of storing the digital representation in a memory.

14. The method of claim 13 further comprising the step of reading the digital representation from the memory prior to step b.

15. A video graphics subsystem having on-screen display insertion means for converting a video signal from an analog source signal to a digital signal, combining graphics information with the digital signal to form a composite signal, and converting the composite digital signal to an analog video output signal coupled to a display, the subsystem being characterized by:

a bypass having a controllable switch for coupling the analog source signal directly to the display.

16. The video graphics subsystem recited in claim 15 wherein the bypass comprises a switch.

17. The video graphics subsystem recited in claim 15 wherein the switch is controlled by a microprocessor such that the bypass is deactivated during intervals when graphics information is desired and the bypass is activated during intervals when graphics information is not desired.

18. The video graphics subsystem recited in claim 15 further comprising a memory for storing the graphics information.

19. The video graphics subsystem recited in claim 18 further comprising a microprocessor for generating and storing the graphics information in the memory.

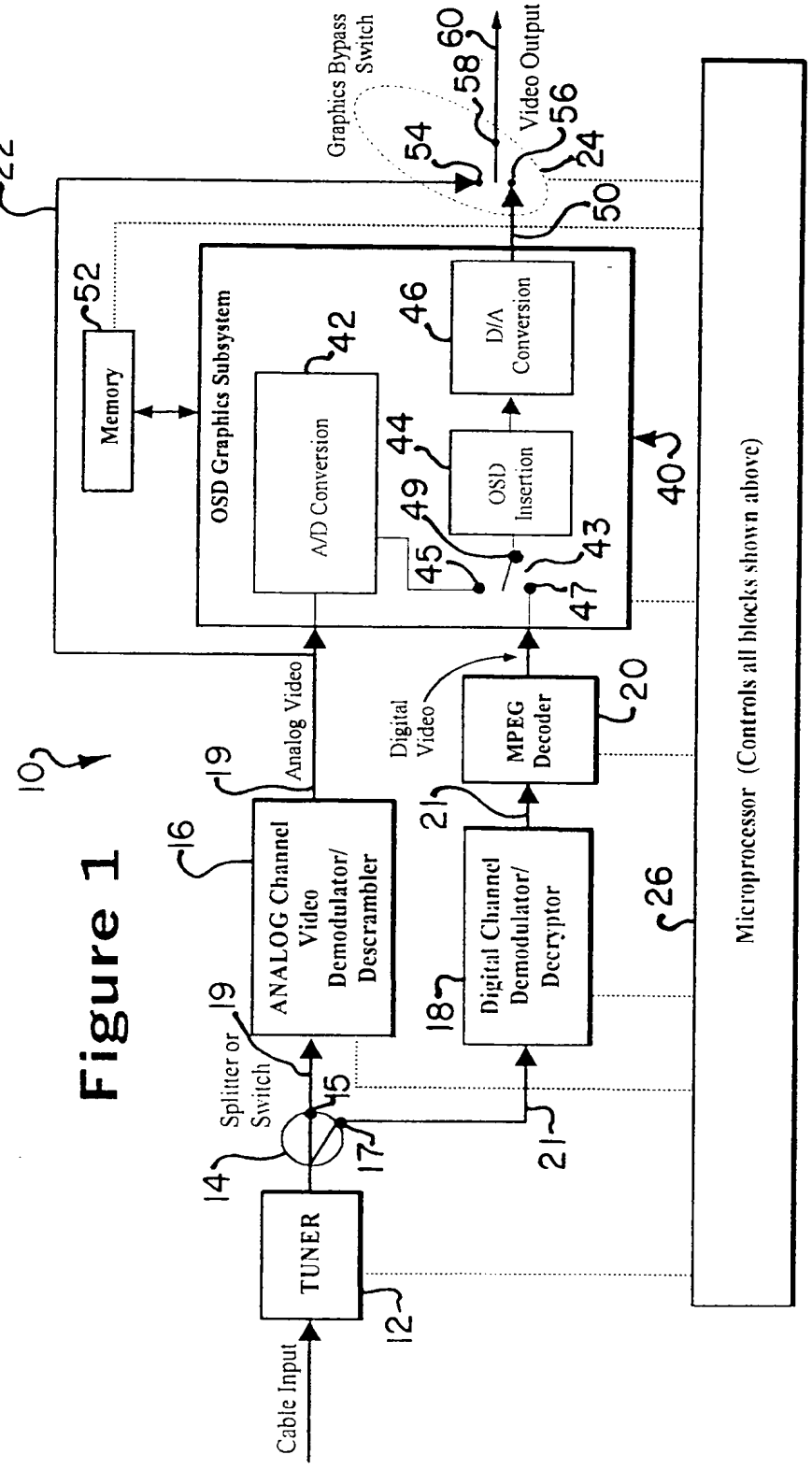
Graphics Bypass Switch
Video Output
Memory
OSD Graphics Subsystem
A/D Conversion
D/A Conversion
OSD Insertion
Analog Video
Digital Video
MPEG Decoder
ANALOG Channel Video Demodulator/ Descrambler
Digital Channel Demodulator/ Decryptor
Splitter or Switch
TUNER
Cable Input
Microprocessor (Controls all blocks shown above)
10
12
14
15
16
17
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Figure 1

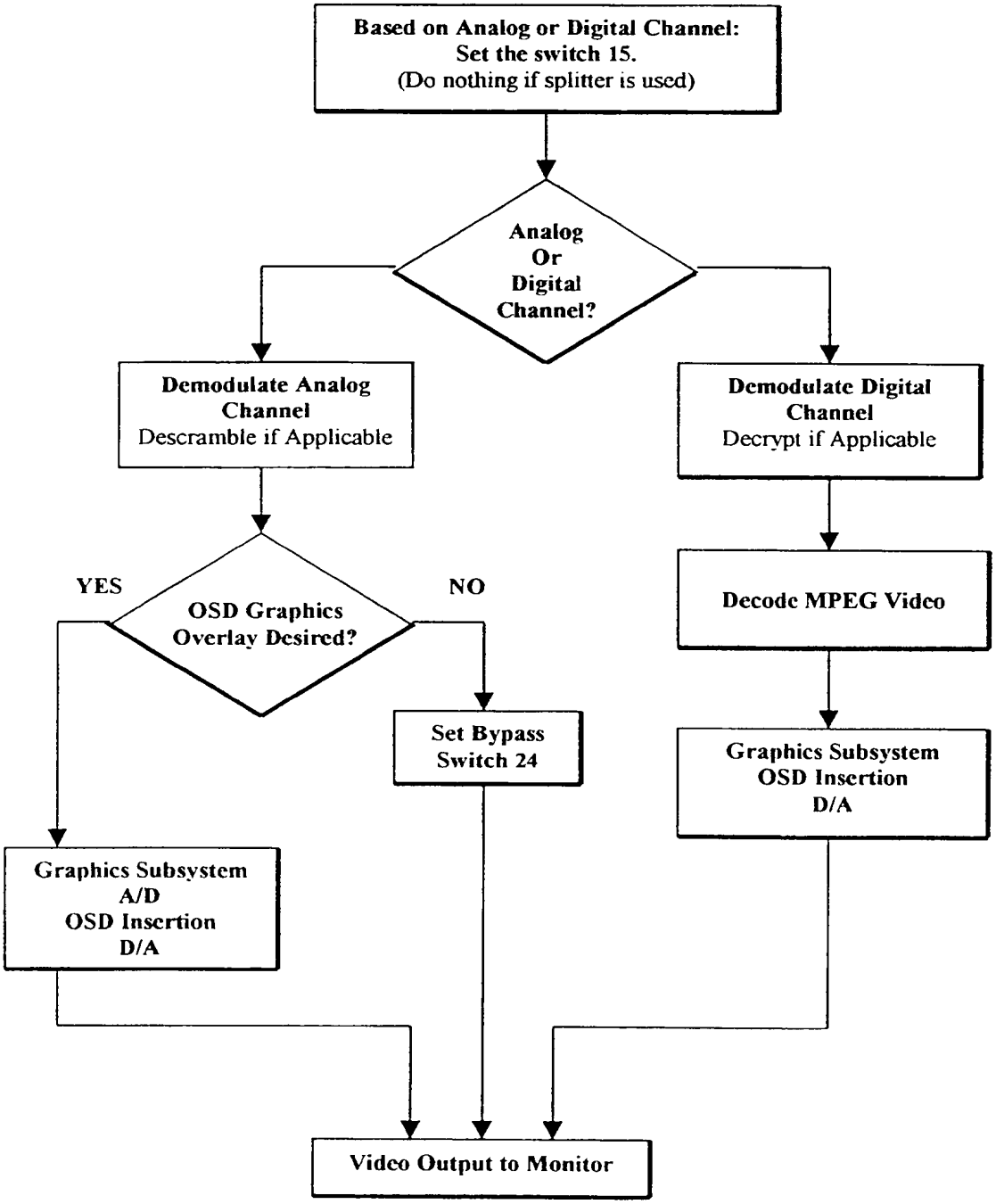
Based on Analog or Digital Channel:
Set the switch 15.
(Do nothing if splitter is used)
Analog
Or
Digital
Channel?
Demodulate Analog
Channel
Descramble if Applicable
Demodulate Digital
Channel
Decrypt if Applicable
YES
OSD Graphics
Overlay Desired?
NO
Decode MPEG Video
Set Bypass
Switch 24
Graphics Subsystem
OSD Insertion
D/A
Graphics Subsystem
A/D
OSD Insertion
D/A
Video Output to Monitor

Figure 2

INTERNATIONAL SEARCH REPORT

Interi nal Application No
PCT/US 99/22305

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04N5/445

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 701 367 A (THOMSON CONSUMER ELECTRONICS) 13 March 1996 (1996-03-13) the whole document ---	1,3-5,7, 11-13, 15,18
A	GB 2 326 551 A (DAE WOO ELECTRONICS CO LTD) 23 December 1998 (1998-12-23) page 9, line 15 -page 11, line 20 page 12, line 9 -page 15, line 19; figures 2-4C ---	1,7,11, 15
A	US 5 638 112 A (BESTLER CAITLIN B ET AL) 10 June 1997 (1997-06-10) the whole document --- -/--	1,7,11, 15

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 May 2000	19/05/2000

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/US 99/22305

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 541 666 A (ZHU QIANG ET AL) 30 July 1996 (1996-07-30) cited in the application column 2, line 43 -column 4, line 5; figure 1	1,7,11, 15

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Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

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